RTL FPGA synthesis manual

0pf.org Jun/19/2015

(2 pages)

(*1)Hardware and software requirement

(1.1) Hardware

* Computer running X86 Linux having USB port

(ref 0pf environment, Mac OS 10.9.5, Oracle Virtual Box 4.3.10 r93012, OpenSuSE i686, Xwindow on OpenSuSE)

(allocate 1GB memory to virtual Box)

* Xilinx Spartan-6 FPGA LX9 Microboard (it is not necessary during synthesis, it is necessary after synthesis, program the bitstream)

(1.2) Software

* Xilinx ISE

(ref 0pf environment, ISE 13.1)

* SH2 development tools:

sh2-elf-gcc, sh2-elf-ld, sh2-elf-ar, sh2-elf-ranlib, sh2-elf-objcopy

(ref 0pf environment, sh2-elf-gcc: 4.6.0 (GCC), sh2-elf-ld: GNU Binutils 2.21,)

* perl

(*2) Operation of synthesis

(2.1) setup Xilinx synthesis tool

(ref 0pf environment Xilinx ISE_WebPACK, place "Xilinx.lic" at ~/.Xilinx)

(2.2) set path of sh2 tools

for example, set path = ($path /opt/toolchains/SH2/bin) in ~/.cshrc

(2.3) download soc_top-${yyyymmdd}.tar and expand to your design directory

As expand result, it has a top directory soc_top (referred from now ${soc_top}

(2.4) make genram and test

```
cd ${soc_top}/tools/genram
 make
cd ${soc_top}/tools/test
 make
```

(2.5) Xilinx environment set

execute a proper setting

0pf environment, "`source /opt/Xilinx/13.1/ISE_DS/settings32.sh`"

for bash (shell)

"`source /opt/Xilinx/13.1/ISE_DS/settings32.sh`" for C shell

(2.6) synthesis

```
cd ${soc_top}
make microboard
```

(2.7) After six minutes (depending to the computer environments) synthesis finishes.

On ${soc_top}/output/${date_time}_microboard

microboard9.bit, microboard9.msc

are generated, those are bitstream for LX9 microboard.

(*3) After synthesis

Refer 0pf.org "LX9 Bitstream flush program and run manual" to program LX9 microboard.

There are two ways.

1. Using single file (microboard9.bit) and do all procedures.
2. Using two files (microboard9.bit, microboard9.mcs) that makes unnecessary to generate ".mcs" file.

`End of RTL FPGA synthesis manual`